Patents by Inventor Viswanadam Gautham

Viswanadam Gautham has filed for patents to protect the following inventions. This listing includes patent applications that are pending as well as patents that have already been granted by the United States Patent and Trademark Office (USPTO).

- **Micro-device on glass**

  Patent number: 8911636

  Abstract: A method of fabricating a micro-device having micro-features on glass is presented. The method includes the steps of preparing a first glass substrate, fabricating a metallic pattern on the first glass substrate, preparing a second glass substrate and providing one or more apertures on the second glass substrate, heating the first glass substrate and the second glass substrate with a controlled temperature raise, bonding the first glass substrate and the second glass substrate by applying pressure to form a bonded substrate, wherein the metallic pattern is embedded within the bonded substrate, cooling the bonded substrate with a controlled temperature drop and thereafter maintaining the bonded substrate at a temperature suitable for etching, etching the metallic pattern within the bonded substrate, wherein an etchant has access to the metallic pattern via the apertures, forming a void within the bonded substrate, wherein the void comprises micro-features.

  Type: Grant

  Filed: September 29, 2013

  Date of Patent: December 16, 2014

  Inventor: Viswanadam Gautham

- **MICRO-DEVICE ON GLASS**

  Publication number: 20140054261

  Abstract: A method of fabricating a micro-device having micro-features on glass is presented. The method includes the steps of preparing a first glass substrate, fabricating a metallic pattern on the first glass substrate, preparing a second glass substrate and providing one or more apertures on the second glass substrate, heating the first glass substrate and the second glass substrate with a controlled temperature raise, bonding the first glass substrate and the second glass substrate by applying pressure to form a bonded substrate, wherein the metallic pattern is embedded within the bonded substrate, cooling the bonded substrate with a controlled temperature drop and thereafter maintaining the bonded substrate at a temperature suitable for etching, etching the metallic pattern within the bonded substrate, wherein an etchant has access to the metallic pattern via the apertures, forming a void within the bonded substrate, wherein the void comprises micro-features.

  Type: Application
  Filed: September 29, 2013
  Publication date: February 27, 2014
  Inventor: Viswanadam Gautham

- **Method for packaging a semiconductor device**

  Patent number: 7344917

  Abstract: A method for packaging a semiconductor device includes forming through holes (12) in a base substrate (10) and depositing a conductive material (14) on a first side (16) of the base substrate (10) to form a conductive layer (18) such that the conductive material (14) fills the through holes (12). The conductive layer (18) is patterned and etched to form interconnect traces and pads (22). Conductive supports (24) are formed on the pads (22) such that the conductive supports (24) extend through respective ones of the through holes (12).

  Type: Grant
  Filed: November 30, 2005
  Date of Patent: March 18, 2008
  Assignee: Freescale Semiconductor, Inc.
  Inventor: Viswanadam Gautham

- **METHOD OF FORMING A TRACE EMBEDDED PACKAGE**

  Publication number: 20070281393

  Abstract: A method of forming a semiconductor package (32) includes etching a conductive sheet (10) to form a first interconnection system (12). An integrated circuit (IC) die (22) is placed on and electrically connected to the first interconnection system (12). Next, a molding operation is performed to encapsulate the IC die (22), the electrical connections (24, 26) and at least a portion of the first interconnection system (12). A portion (20) of the conductive sheet (10) is then removed to expose a surface (30) of the first interconnection system (12). A second interconnection system (34) then is formed over the exposed surface (30) of the first interconnection system (12).

  Type: Application
  Filed: May 30, 2006
  Publication date: December 6, 2007
  Inventors: Viswanadam Gautham

- **Method for packaging a semiconductor device**

  Publication number: 20070122940

  Abstract: A method for packaging a semiconductor device includes forming through holes (12) in a base substrate (10) and depositing a conductive material (14) on a first side (16) of the base substrate (10) to form a conductive layer (18) such that the conductive material (14) fills the through holes (12). The conductive layer (18) is patterned and etched to form interconnect traces and pads (22). Conductive supports (24) are formed on the pads (22) such that the conductive supports (24) extend through respective ones of the through holes (12).

  Type: Application
  Filed: November 30, 2005
  Publication date: May 31, 2007
  Inventor: Viswanadam Gautham

- **Method of making reinforced semiconductor package**

  Patent number: 7160798

  Abstract: A method of making a reinforced semiconductor package includes forming a semiconductor interconnect tablet (24). Formation of the tablet includes providing a plurality of conductive metal tabs (10), positioning a first end (12) of the tabs (10) in a first section of a mold chase (14), positioning a second section of the mold chase (16) over a second end (18) of the tabs (10), such that the tabs (10) are anchored between the first and second sections (14, 16) of the mold chase, loading the first and second sections (14, 16) of the mold chase into a molding system (20) and performing a molding operation such that a plastic mold compound (22) is formed around the metal tabs (10) and an interconnect tablet (24) is formed. Then the first and second sections (14, 16) of the mold chase are removed from the molding system (20) and the interconnect tablet (24) is removed from the first and second sections (14, 16) of the mold chase.

  Type: Grant
  Filed: February 24, 2005
  Date of Patent: January 9, 2007
  Assignee: Freescale Semiconductor, Inc.,
  Inventors: Viswanadam Gautham,

- **Method of making reinforced semiconductor package**

  Publication number: 20060189120

  Abstract: A method of making a reinforced semiconductor package includes forming a semiconductor interconnect tablet (24). Formation of the tablet includes providing a plurality of conductive metal tabs (10), positioning a first end (12) of the tabs (10) in a first section of a mold chase (14), positioning a second section of the mold chase (16) over a second end (18) of the tabs (10), such that the tabs (10) are anchored between the first and second sections (14, 16) of the mold chase, loading the first and second sections (14, 16) of the mold chase into a molding system (20) and performing a molding operation such that a plastic mold compound (22) is formed around the metal tabs (10) and an interconnect tablet (24) is formed. Then the first and second sections (14, 16) of the mold chase are removed from the molding system (20) and the interconnect tablet (24) is removed from the first and second sections (14, 16) of the mold chase.

  Type: Application
  Filed: February 24, 2005
  Publication date: August 24, 2006
  Inventors: Viswanadam Gautham

Integrated circuit device and method of manufacturing thereof

Abstract

A method of manufacturing an integrated circuit (IC) device is disclosed. A wafer including multiple dies is processed to form solder bumps at the bond pad locations. A conductive substrate is patterned for routing traces and connection pads and partially etched. Routers are formed to electrically route a connection pad to the interior of its corresponding routing terminals. The etched connection pads corresponds to the plurality of bond pad locations of the IC chip. The bumped IC chip is aligned and attached to the conductive substrate through the connection pads and solder bumps. The attached IC chip and the first side of the conductive substrate are

then encapsulated. Un-processed conductive material is then removed from a second side of the substrate, opposite the first side, to expose the routers and routing terminals. Contacts are formed on the second side of the substrate that electrically connect with the routers in the interior of the connection pads to thereby electrically connect with the connection terminals on the first side of the IC chip. The packaged IC are then separated along the separation lines to produce individualized dies. An IC device including a separated die is also disclosed.

Type: Application
Application PCT/SG2005/000225 events
2005-07-09
Application filed by Gautham Viswanadam
2005-07-09
Priority to PCT/SG2005/000225
2007-01- 18
Publication of WO2007008171A2
2007-06-07
Publication of WO2007008171A3
Inventors: Viswanadam Gautham

Method for packaging a semiconductor device
Patent: US20070122940A1
Abstract
A method for packaging a semiconductor device includes forming through holes (**12**) in a base substrate (**10**) and depositing a conductive material (**14**) on a first side (**16**) of the base substrate (**10**) to form a conductive layer (**18**) such that the conductive material (**14**) fills the through holes (**12**). The conductive layer (**18**) is patterned and etched to form interconnect traces and pads (**22**). Conductive supports (**24**) are formed on the pads (**22**) such that the conductive supports (**24**) extend through respective ones of the through holes (**12**).
Application US11/290,300 events
Publication of US20070122940A1
2008-03-18
Application granted
2008-03-18
Publication of US7344917B2
2019-11-10
Application status is Active
2026-02-09

Method for packaging a semiconductor device
Patent number: 7344917
Abstract: A method for packaging a semiconductor device includes forming through holes (12) in a base substrate (10) and depositing a conductive material (14) on a first side (16) of the base substrate (10) to form a conductive layer (18) such that the conductive material (14) fills the through holes (12). The conductive layer (18) is patterned and etched to form interconnect traces and pads (22). Conductive supports (24) are formed on the pads (22) such that the conductive supports (24) extend through respective ones of the through holes (12).

Type: Grant
Filed: November 30, 2005
Date of Patent: March 18, 2008
Assignee: Freescale Semiconductor, Inc.
Inventor: Viswanadam Gautham

METHOD OF FORMING A TRACE EMBEDDED PACKAGE
Publication number: 20070281393
Abstract: A method of forming a semiconductor package (32) includes etching a conductive sheet (10) to form a first interconnection system (12). An integrated circuit (IC) die (22) is placed on and electrically connected to the first interconnection system (12). Next, a molding operation is performed to encapsulate the IC die (22), the electrical connections (24, 26) and at least a portion of the first interconnection system (12). A portion (20) of the conductive sheet (10) is then removed to expose a surface (30) of the first interconnection system (12). A second interconnection system (34) then is formed over the exposed surface (30) of the first interconnection system (12).
Type: Application
Filed: May 30, 2006
Publication date: December 6, 2007
Inventors: Viswanadam Gautham

Method of making reinforced semiconductor package
Patent number: 7160798
Abstract: A method of making a reinforced semiconductor package includes forming a semiconductor interconnect tablet (24). Formation of the tablet includes providing a plurality of conductive metal tabs (10), positioning a first end (12) of the tabs (10) in a first section of a mold chase (14), positioning a second section of the mold chase (16) over a second end (18) of the tabs (10), such that the tabs (10) are anchored between the first and second sections (14, 16) of the mold chase, loading the first and second sections (14, 16) of the mold chase into a molding system (20) and performing a molding operation such that a plastic mold compound (22) is formed around the metal tabs (10) and an interconnect tablet (24) is formed. Then the first and second sections (14, 16) of the mold chase are removed from the molding system (20) and the interconnect tablet (24) is removed from the first and second sections (14, 16) of the mold chase.
Type: Grant
Filed: February 24, 2005
Date of Patent: January 9, 2007
Assignee: Freescale Semiconductor, Inc.
Inventors: Viswanadam Gautham

Method of making reinforced semiconductor package
Publication number: 20060189120
Abstract: A method of making a reinforced semiconductor package includes forming a semiconductor interconnect tablet (24). Formation of the tablet includes providing a plurality of conductive metal tabs (10), positioning a first end (12) of the tabs (10) in a first section of a mold chase (14), positioning a second section of the mold chase (16) over a second end (18) of the tabs (10), such that the tabs (10) are anchored between the first and second sections (14, 16) of the mold chase, loading the first and second sections (14, 16) of the mold chase into a molding system (20) and performing a molding operation such that a plastic mold compound (22) is formed around the metal tabs (10) and an interconnect tablet (24) is formed. Then the first and second sections (14, 16) of the mold chase are removed from the molding system (20) and the interconnect tablet (24) is removed from the first and second sections (14, 16) of the mold chase.
Type: Application
Filed: February 24, 2005
Publication date: August 24, 2006
Inventors: Viswanadam Gautham